n*16 bit inputs

| | 0 | 4 | 6 | 2 | 8 | 12 | 13 | 10 |
|---|---|---|---|---|---|---|---|---|
| CLK$_0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CLK$_1$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| CLK$_2$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| CLK$_3$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

n=1
n=2

n*20 bit inputs

| | 0 | 4 | 6 | 3 | 1 | 8 | 12 | 13 | 11 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|
| CLK$_0$ | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| CLK$_1$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| CLK$_2$ | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| CLK$_3$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

n=1
n=2

serial output data 86

3RD mux module 100

serial data clock 110

2ND mux module 98

1 4 2

1 4 4

intermediate data clock 108

4

1ST mux module 96
(4 - 16:1 muxes)

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

CLK$_0$
CLK$_1$
CLK$_2$
CLK$_3$

4

[3:0]
[19:16]
[15:12]
[7:4]
[11:8]
[23:20]
[39:36]
[35:32]
[27:24]
[31:28]

TX parallel data 48
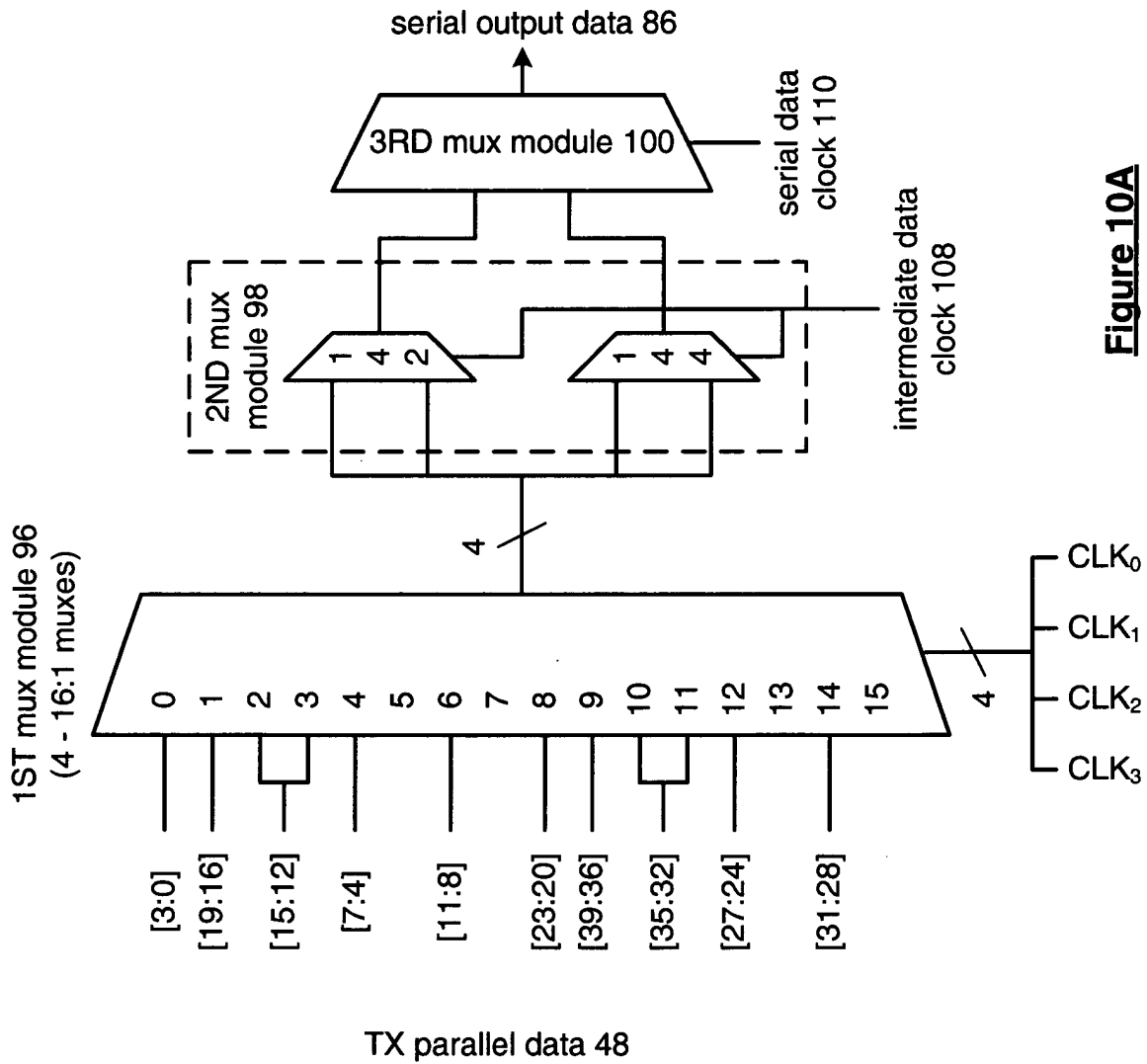
**Figure 10A**
**parallel to serial module 84**

serial output data 86

3RD mux module 100

serial data clock 110

2ND mux module 98

intermediate data clock 108

1 4 2

1 4 4

162

163

164

4

1ST mux module 96
(4 - 16:1 muxes)

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

CLK₀

CLK₁

CLK₂

CLK₃

4

[3:0]
[19:16]
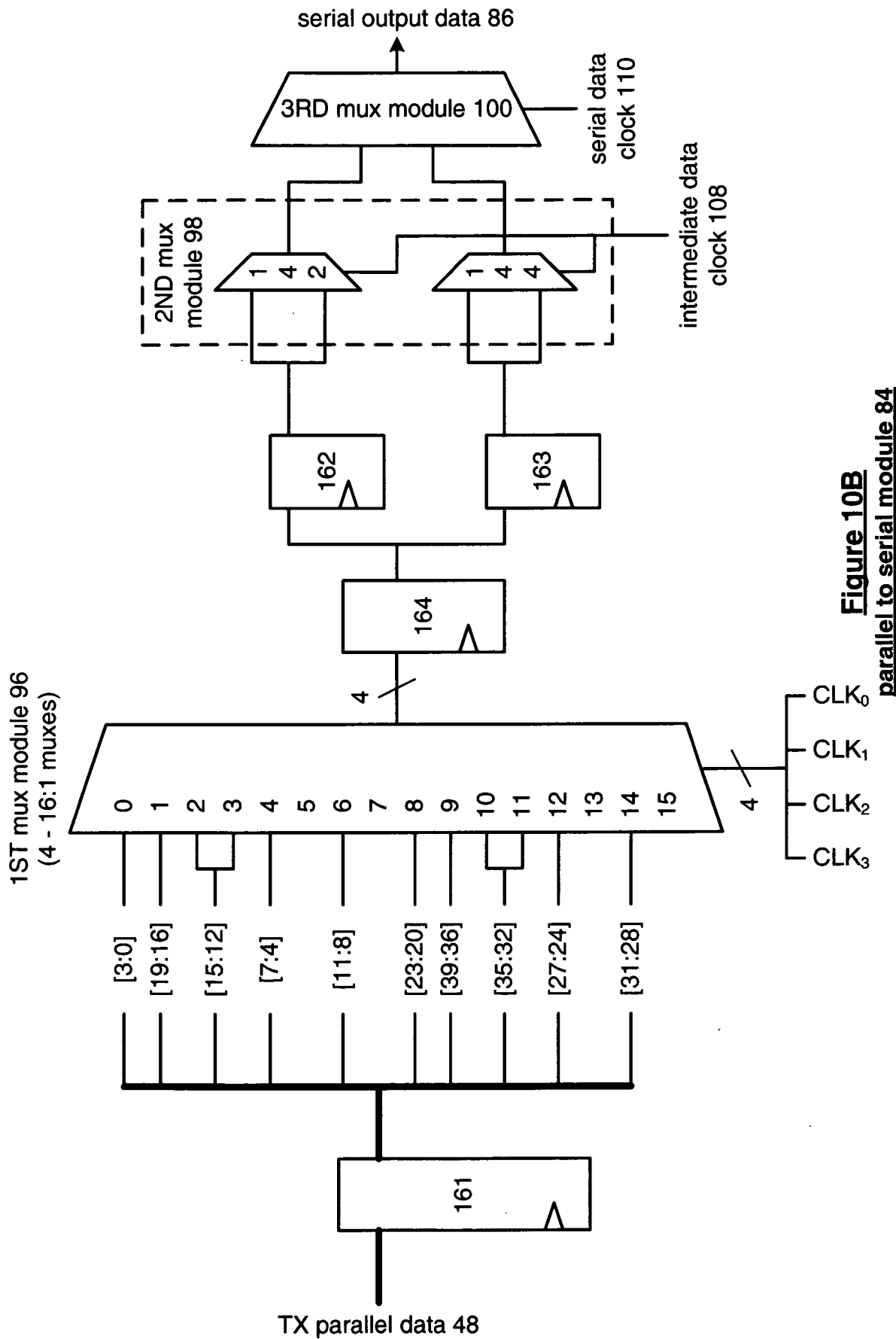[15:12]
[7:4]
[11:8]
[23:20]
[39:36]
[35:32]
[27:24]
[31:28]

161

TX parallel data 48

**Figure 10B**
parallel to serial module 84